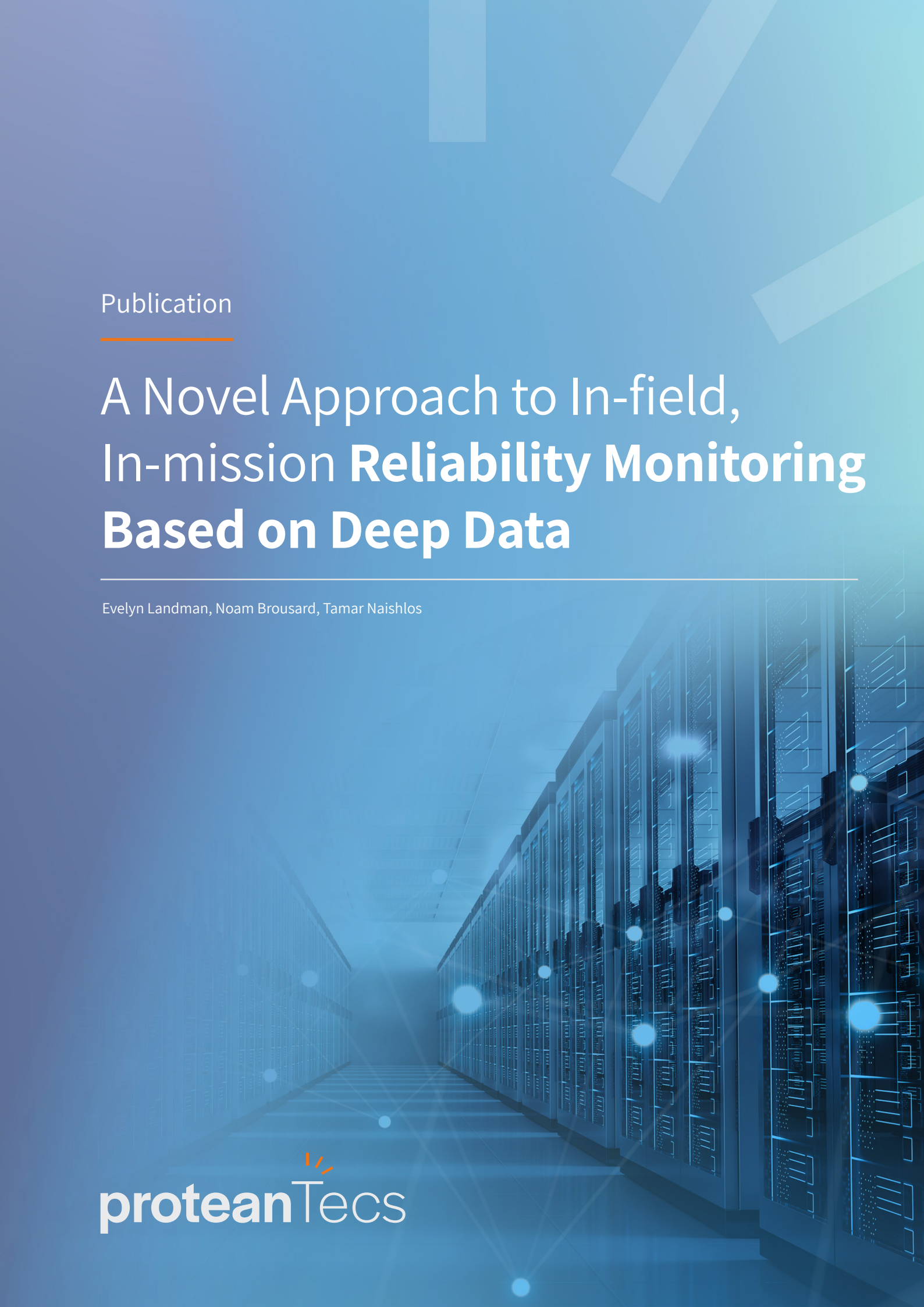
Publication

A Novel Approach to In-field, In-mission **Reliability Monitoring Based on Deep Data**

Evelyn Landman, Noam Brousard, Tamar Naishlos



proteanTecs

A Novel Approach to In-field, In-mission Reliability Monitoring Based on Deep Data

Digital Object Identifier: 10.1109/IRPS45951.2020.9128846

URL: https://ieeexplore.ieee.org/document/9128846

A Novel Approach to In-field, In-mission Reliability Monitoring Based on Deep Data

ABSTRACT

This paper describes a Deep Data approach to reliability monitoring in advanced electronics, based on degradation as a precursor for failure. By applying machine learning algorithms and analytics to data created by on-chip monitoring IPs (Agents), IC/system health and performance can be continuously monitored, at all stages of the product lifecycle. Realtime degradation analysis of critical parameters and failure mechanisms, under field conditions and application environments, points to the underlying Physics of Failure, which in turn allows to estimate the time to failure. Users are alerted on faults in advance, via a cloud-based analytics platform, and can take corrective action to prevent failures. The future of reliability physics and engineering is fundamentally shifting from accelerated lifetime tests to in-field failure prediction.

Keywords- Deep Data, degradation monitoring, on-chip monitoring, BTI, EM, Stress Migration, software, analytics platform, Margin Agents, Profiling Agents, Workload Agents, High Bandwidth Memory (HBM), machine learning, predictive mantainance, relability, Idsat, Vth, Ioff, HTOL, integrated circuits (IC), physics of failure.

I. INTRODUCTION

All materials tend to degrade, and will eventually fail, with time. The evidence of material device degradation is apparent in nature. A fresh coating of paint on a house will eventually crack and peel. Doors in a house can become stuck due to the shifting of the foundation. The new finish on an automobile will oxidize over time [1]. Electronics are no exception to that rule.

During the infancy of the modern semiconductor industry, the 'conventional belief' was that solid-state components would be free of any reliability issues, due to the absence of any 'moving parts.' Experience over the last few decades has shown this belief to be overly optimistic. Management of reliability is one of the key semiconductor engineering concerns, especially when dealing with complex high component counts, or systems subject to extreme environmental conditions [2].

II . RELIABILITY IN FACE OF COMPLEXITY

The steady march of Moore's Law in semiconductors, the core components of electronics, has enabled the creation of ever more complex systems at all levels – die, IC, board and package. Today's devices can contain billions of transistors and integrate a wide variety of previously discrete components and independent systems. With the arrival of fin-FETs, metal gate, low-k dielectric and other advanced process nodes, devices are getting even smaller. Packaging complexity is also growing, with options including SIP, MCM, stacked die, TSV and Cu wire [3]. 3D IC integration, in which thin chips/interposers are stacked in the third dimension with through-silicon vias and micro bumps, enables high performance and density, low power consumption, wide bandwidth, small form factor, and light weight [4]. Meanwhile, the materials, coatings and molding compounds associated with advanced packages and boards are also growing more complex [3]. These advancements enable the scale required to meet modern demands. Systems today are finding new applications and winding their way ever deeper into our daily lives. This trend is expected to continue at an accelerated pace as exemplified by smart cars, homes, cities, factories, healthcare, agriculture, etc. loosely aggregated under the umbrella term internet-of-things (IoT) and enabled by high-data-rate 5G wireless communications [5]. This is magnified by the mass move of data, logic and applications to the Cloud. As demands and dependencies escalate, so does the need for uncompromising reliability. System failures can bear heavy financial loss and, in some cases, even loss of life. Abrupt service interruption, costly downtime and product delays or recalls cause devastating reputational damage for brand owners. It is important to find and fix failures before they occur, but to do this a predictive approach must be systematically implemented by service providers and their supply chains.

III. THE PHYSICS OF FAILURE

The reliability of an electronic system over time can be described as a bathtub curve, as shown in **Fig. 1.** There are three distinct reliability regions associated with this curve. First, during the early stages of device

use, the failure rate is relatively high, and this region is referred to as the early failure rate (EFR) region. The failures occurring in the EFR region are generally due to rather gross defects. Second, after the initial high EFR portion of the curve, a much lower and stable failure rate occurs, and this region is referred to as the intrinsic failure rate (IFR) region. The IFR fails can be due to very small defects in the materials. After the IFR region, one usually has a region of rapid turn-up in the failure rate which is referred to as the wear-out region. The wear-out region is driven by normal material/ device degradation. This wear-out region is strongly dependent of the level of stress and temperature [1].

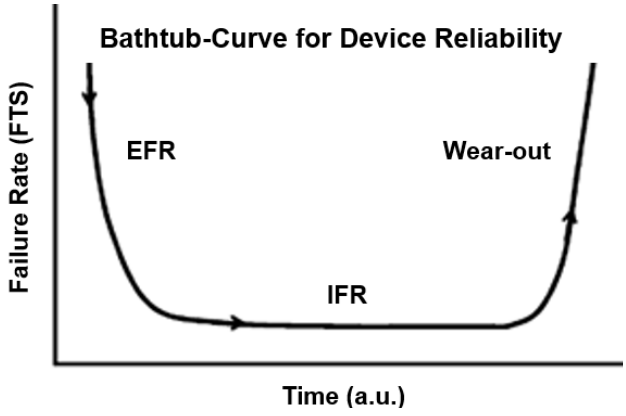


Figure 1: Bathtub reliability curve

Principal failure mechanisms associated with modern ICs are affected by the design, manufacturing process, use conditions, and the interaction between the three. Critical parameters associated with microelectronics (threshold voltages, drive currents, interconnect resistances, capacitor leakages, etc.) will degrade with time, before reaching the tipping point of failure. Mechanisms that demonstrate degradation prior to failure include bias temperature instability (BTI), hot carrier injection (HCI), surface inversion (SI), electro-migration (EM), stress-migration (SM), temperature cycling fatigue and corrosion [1].

In order to understand the lifetime of the device, it is important to understand the reliability physics (kinetics) for each of the potential failure mechanisms [1] and then employ a monitoring method that can be used to predict, minimize, and analyze the occurrence of device failures. A Physics-of-Failure (PoF) methodology can be used to model the effect of these factors and provide guidance to control them for maximum reliability. Time-to-failure depends on the amount of degradation that can be tolerated in some critically important device parameter [1]. By understanding the possible failure mechanisms, continuously monitoring degradation and factoring in time-to-failure, electronics manufacturers and companies deploying them can take corrective action in advance and prevent system failures in the field.

IV . DESIGN-IN VS. TEST-IN RELIABILITY

Quality requirements have become increasingly stringent, specified in terms of initial or “time zero” quality as well as product reliability, both typically using the metric of defective parts per million or DPPM. Targets for both time zero and reliability DPPMs are continually being driven downward [6]. The ‘conventional methodology’ for management of IC reliability dictates that component reliability is to be empirically demonstrated through accelerated life tests – i.e., tests at elevated temperature and/ or voltage, extreme mechanical stress during thermal cycling. If a reliability issue is found during these tests, the circuit is redesigned or the manufacturing process is changed, and the product is tested again [2]. Even with the ever-growing number of tests and a test often being applied multiple times under different electrical/ environmental conditions, test escapes exist [7]. These can be either a time-zero issue or a ‘walking wounded’ device that carries enhanced reliability risks with no externally visible or parametric evidence of a problem. Additional testing limitations include under sampling or random sampling, limited coverage, and the lack of ability to detect marginal defects.

Quality escapes coupled with inherent device-degradation during operation dictate a need to move the reliability management practices beyond the current ‘standard’ approaches [2]. Achieving a zero failure-rate using conventional reliability testing is impossible; since either the sample size, acceleration factor, or test time must go to infinity [1]. Best-in-class companies are consequently developing a set of new practices, based on the PoF, reliability statistics, and an understanding of interactions between the design and process attributes, in order to manage reliability throughout the IC product life cycle [2].

When deployed in the field and operating in their respective application, electronics today offer limited visibility into the actual state of the system. Best known methods depend on inferential monitoring of a wide variety of sensors in the best case, and on pure statistics in the worst. Consequentially, nowadays electronics service providers must rapidly and effectively deal with failure after it happens or be overly cautious (redundancies, regular upgrades, replacements and service). In both cases, there is a price tag.

Continuous monitoring of ICs using Deep Data designed into the system is a paradigm shift in reliability – transferring the focus from predicting device failure rates to predicting device failure.

V. ON-CHIP MONITORING WITH PROTEUS

To get a deeper, more accurate and insightful view into electronics, there is a need for Deep Data from the very chips at the core of the systems.

Providing an emerging approach to reliability assurance, Proteus™ is a platform that provides valuable visibility and actionable insight into electronics. It monitors ICs and the systems embedding them throughout the lifecycle of design, characterization, qualification, production and during in-field operation, to guarantee the strict quality and reliability requirements of advanced technology applications. Proteus extracts, monitors and correlates past, present and (predicted) future information on the electronic system to report on its health and performance at every stage. It improves quality during production and when in-field – detects degradation, diagnoses faults and predicts failures and remaining useful life. Accurate prediction allows system operation, with the possibility of planning scheduled maintenance at the most convenient and inexpensive time. The benefits are service reliability and availability, increased system lifetime, increased safety and lower maintenance costs.

Proteus comprises custom IPs called Agents™ embedded into ICs and a cloud-based analytics platform that reads and interprets the Agent data throughout the various stages of the product lifecycle, from design to field.

The Agents mimic the design and monitor key electrical parameters and circuits in the IC and the system that it is embedded in, during test and during normal operation, exposing essential, critical, Deep Data that is not accessible today. A suite of Agents monitors different electrical parameters and parts of the design and together they provide a high coverage of an IC/system's parametric behavior from many angles.

The Proteus platform, which comes uploaded with millions of simulations representing the Agents and the design expected results, reads and processes the unique Agent measurements and applies machine learning estimators, algorithms and advanced analytics to the data. This data and inferences are the basis for providing both high visibility and actionable insights. The enhanced visibility provides a detailed performance report of the IC, rooted in the actual circuitry, per application running on it, per environment circumstances. The solution is 'in-situ', non-intrusive and operates in mission mode. All the machine learning algorithms and the analytics are performed in the Proteus platform once the data is uploaded.

Since Proteus is active not only while the product is in use, but also throughout the various stages of its production testing, the Agent information, relevant data and insights from different production stages are accumulated and leveraged for improved insight post-launch – enabling reduction of unnecessary margins, increased visibility and coverage, predictive health alerts and significant overall financial savings. During production stages, Proteus provides unprecedented visibility, which is translated into quality and parametric yield improvements.

Proteus provides a 'must be' path for advanced electronics to provide predictive health, i.e. failure prevention during its operational lifetime. It also presents a new level of visibility into the power/performance implications of running actual applications on the product.

The Proteus Agents and platform have already been deployed in various process technologies and key industry sectors, for test chips as well as for production chips. They are silicon proven in advanced process nodes including 28nm, 16nm and 7nm, and different flavors of these process technologies.

The pictures and graphs presented in this paper show silicon data as viewed in the Proteus analytics platform. In order to adhere to customer confidentiality

requirements, the figures do not include real silicon data, but an accurate representation of how the data was seen in order to demonstrate the capability of the solution described.

VI. PROTEUS AGENTS

A. Margin Agents (MAs)

MAs are low gate count, low power consumption circuits that continuously and simultaneously measure the timing margin (or maximum path delay) at the input of groups of (32, 64) Flip Flops and report the lowest margin found among them, as shown if **Fig. 2.** The MA measures the setup margin to the operating frequency at time zero and the margin reduction due to increase in delay of combinatorial logic or memory outputs converging to these FFs, caused by aging and other reliability issues, latent defects that manifest after stress, etc. The logic used to decide to which Flops to connect these MAs during design ensures a high return on investment from the instance coverage point of view. In addition to designer explicitly requested Flops to be tracked, Proteus algorithms decide on the best FFs to connect to, taking into account various metrics such as choosing Flops with the highest logic fan-in to maximize coverage, as well as choosing Flops that terminate paths with highest likelihood of being frequency limiting when considering the full process variation, over a wide range of temperatures and voltages, all while employing as low a number of MAs as possible to minimize area cost incurred.

This allows high visibility into the chip performance and its interaction with the applications and environmental stress, hot spots and local I/R drop effects localization, parametric coverage and stress correlation between tests/applications.

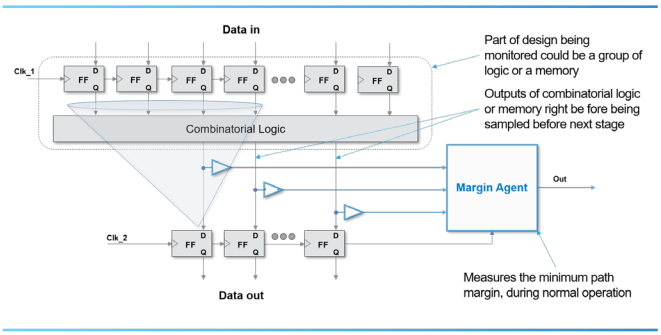


Figure 2: Margin Agent connected to and monitoring a design/circuit

The Proteus platform introduces the “Margin Maps” concept to analyze the margin or path delay inside blocks in the IC per clock domain of interest, as shown in **Fig. 3.** In Fig. 3 a specific block inside an IC is shown, X and Y coordinates are the actual block coordinates and each rectangle is a specific MA, and its color depicts the worst path delay measured for a specific test or system application to the running clock frequency in [ps]. The measurements are done by setting the MAs to monitor during a stress test or application. At the end of the test or application the worst measured margin measured by each MA is extracted from the IC in a digital way through different interfaces such as JTAG or I2C or bridges to a native Advanced Peripheral Bus (APB) protocol supported by the Proteus Agents controller embedded into the IC together with the Proteus Agents.

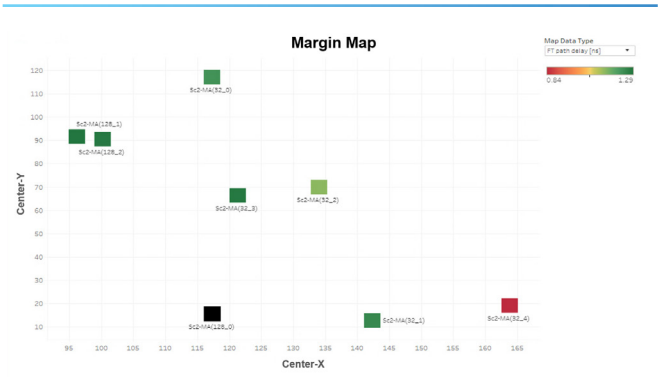


Figure 3: Margin Map of a specific block inside an IC. X axis are the x coordinates of the specific block. Y axis is the Y coordinates of the specific block. Each rectangle is a MA inside the block. The measurements plotted are the worst-case path delay measured for each MA during a specific test; in this case it is a functional stress test during Final Test stage.

B. Profiling and Classification Agents

The Design Profiling Agents (DPAs) are circuits based on standard cells which mimic the specific design, design tools and methods. The Process Classification Agents (PCAs) are custom circuits designed to generate correlative data to the actual transistor electrical parameters and the RC characteristics. These latter Agents, once activated to measure, generate digital data with high correlation to certain electrical parameters, such as Vth, Idsat and Ioff of that IC, and the specific IC area they are placed on. These Agents are capable of distinguishing between sets of electrical parameters of different Vth type, L effective, and MOS type (PMOS and NMOS). The Proteus platform uses pre-loaded simulated data of the Profiling Agents for hundreds of Monte-Carlo corners and many V and T points, this data is used as training data to generate machine learning estimators. This data is also the expected data for the Agents and the design. Based on the Profiling Agent readouts and the machine learning estimators it can infer the electrical process parameters, as well as Monte Carlo corners and RC models that best represent the IC and the IC sub-blocks. These Profiling Agents are used mainly in the production, testing and qualification stages to perform post to pre silicon correlation, and track electrical parameter changes during qualification. Additional significant use cases of these Profiling Agents are an early and fine profiling and classification of the ICs into fine groups called “Families”, a precise segmentation of the production material into same power/ performance groups. This serves as a basis for binning, grading, outlier detection and systematic shifts during production. “Families” are generated using a different type of machine learning algorithms, that use the Agent readouts and pre silicon simulations to classify the ICs into groups that will behave very similarly from the parametric point of view: delay, leakage current, dynamic power and so on, at whatever operating condition (V and T).

C. Operational Agents

The Operational Agents monitor the effects of actual operation of the IC in the system environment; the stress or workload it experiences, the voltage noise, clock characteristics, thermal stress, and other environmental and operation aspects of the IC.

One type of the Operational Agents is of special interest for lifetime reliability applications, the Workload Agent. The Workload Agent provides an integrated stress measure over time, integrating voltage, temperature and toggle rate, into one figure. The higher the voltage, temperature or toggle rate for a specific IC area and clock domain, the higher the figure per time. This information can be used in production to compare different testing environments and the stress (as measure by V/T and Toggle rate) induced into the IC. During lifetime acceleration tests this can be used to correlate degradation to induced stress, and during operational lifetime this can be used as an explanation and correlation for degradation vs. stress. These Agents provide more in-depth insights on top of the Margin Agents. Whereas the Margin Agents show degradation in performance, Operational Agents shed more light on possible system level causes.

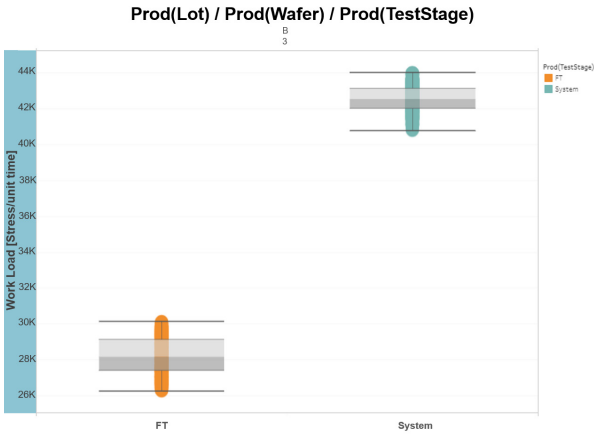


Figure 4: Workload comparison between System Test and ATE Final Test, comparing the stress between different testing environments, for a specific block in an IC and a specific clock domain in the block. Plotting the Workload measured per time for different tests/applications at different environments. In this figure a functional stress test at Final test and a real application at System test. The higher the value means that this block area for the specific clock domain monitored was under higher stress per time. Meaning the higher the voltage and/or the temperature and/or the toggle rate.

D. HBM Agent

The HBM (High Bandwidth Memory) Agent is comprised of an I/O sensor per each of the hundreds of I/O pins, that monitors the Near-End (NE) and Far-End (FE) integrity insights. The NE monitor represents Tx signal quality, derived from the ASIC driver strength, NE micro-bump integrity and interposer integrity. The FE monitor represents Rx signal quality, derived from the DRAM buffer driver strength, FE micro-bump integrity, interposer integrity and the ASIC's Rx buffer sensitivity.

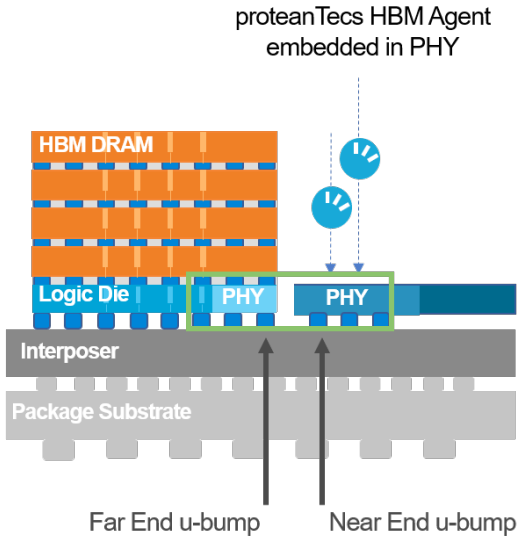


Figure 5: Near End and Far End HBM connectivity integrity measurements

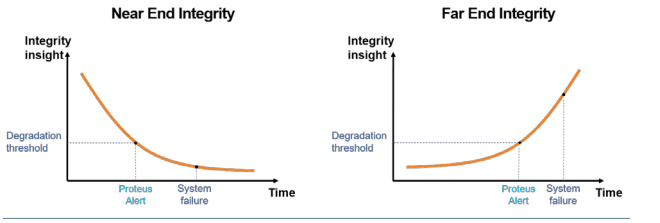


Figure 6: Near End and Far End Integrity alerts

By continuously monitoring signal integrity, Proteus provides actionable insights for reliability monitoring and repair, per pin and in mission mode, to detect degradation trends and avoid failures in-field.

Proteus provides a new method of correlating lane degradation to FE and NE insights, which are functions of ASIC and DRAM driver strength, NE and FE micro-bump integrity, Rx sensitivity and interposer.

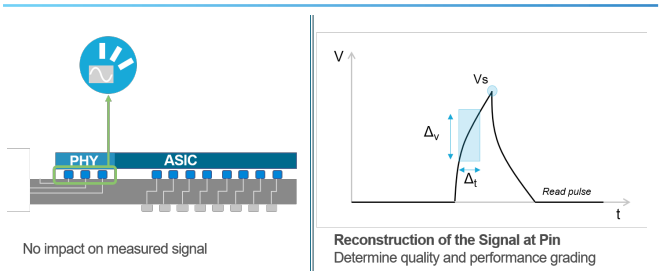


Figure 7: Embedded virtual scope

By alerting on marginal performance of Near-End or Far-End signals, service providers can perform predictive maintenance. Proteus identifies potential candidates for faulty-lane replacement and provides the information to the lane repair mechanism, which replaces marginal lanes with redundant ones at scheduled maintenance cycles. This enables prevention of system failure due to signal quality degradation beyond margin limits.

At system bring-up and characterization, Proteus enables virtual probing of the signal amplitude and slew-rate for each pin, serving as an embedded "scope", without impacting the measured signal. This provides visibility of HBM signal parameters per pin during system characterization, validation and production testing.

VII. DEGRADATION MONITORING: DURING QUALIFICATION AND IN-FIELD

The foundation of the degradation monitoring method is based on the fact that delay or Fmax degradation is a good precursor of failure for many failure mechanisms [8] (see **Fig 8**). By alerting on different evolving degradation patterns, including degradation rate, absolute degradation margin relative to thresholds, time to failure estimation etc., actual failure can be avoided in real life situations.

The Proteus Agent suite includes two Agents that monitor delay degradation at high coverage. The **Margin Agent** constantly and accurately reports margin to the operating frequency of millions of paths in the core of the chip, while the **HBM Agent** reports the delay degradation of an electrical pulse propagation through thousands of advanced package interconnections of the chip to an HBM memory. Together they establish a comprehensive

delay degradation view. They can show how delay degradation is different between different ICs, but also that within the same IC show a non-uniform delay degradation and a dependency. In addition, the degradation can be shown on a delay map which reveals degradation-location dependencies in the IC or in a block in the IC.

The delay degradation rate inspected in the Margin and HBM Agents, as well as the separate degradation rate for PMOS and NMOS transistor inferred electrical parameters based on the PCA readouts and machine learning estimators in the Proteus platform, at lifetime acceleration tests and in-field can shed light on the PoF behind the degradation (NBTI, EM, SM, etc.), and allow optimization of the qualification process and design guard-bands.

By enhancing the qualification stage, the production material is bound to be higher quality, and DPPM is lowered, therefore improving the in-field reliability. During in-field operation alerts on faults before they become failures are set by the Proteus analytics platform, based on the degradation monitoring mechanisms described above.

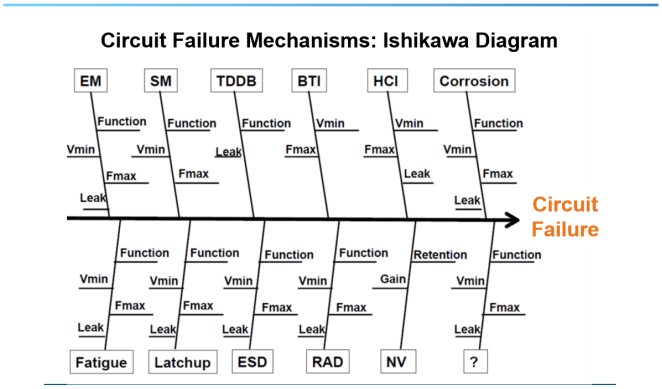


Figure 8: Precursors of failure

VIII. USE CASE: MARGIN AGENT MONITORING

A. Challenge

Visibility at time zero and in-field of millions of internal paths in the IC.

B. Proteus In Action

During lifetime acceleration tests such as HTOL and Burn-In, regularly reading Margin Agents can provide valuable insight into the modelled rate of path delay degradation.

The data collected during these tests enables further conclusions of deeper insights: the margin (delay) degradation rate inspected in the Margin Agents, as well as the separate degradation rate for PMOS and NMOS inferred transistor electrical parameters based on PCAs readouts, at lifetime acceleration tests and operational lifetime can shed light on the physics-of-failure behind the degradation (NBTI, EM, SM, etc.), and allow the optimization of the qualification process and design guard-bands. The same kind of information is available also through the Proteus platform, while the devices and systems are operating in-field. While in-field, different degradation rates may be explained by different causes, not always necessarily a reliability issue. The trends may be affected by reasons other than material degradation. A system may be overstressed, overheated or its clock or voltage supply may not be stable. All these can obscure the rate by which the process is degrading, when analyzing Margin Agent measurements over time. Proteus Operational Agents will constantly monitor the environmental and usage effects on the chip. The Clock Integrity Agent (CIA) and Voltage Integrity Agent (VIA) monitor the clock and voltage supply integrity, respectively. The Noise Modulation Agent measures the “effective cycle time” due to local IR drop and cycle to cycle clock jitter in specific areas of the IC, for specific clock domains. The Workload Agent gauges the stress the chip is experiencing, as represented by an aggregation of temperature, voltage and toggle rate. Local Thermal Agents are small footprint Agents that can easily be dispersed throughout a chip to provide a high coverage thermal map of the chip, highlighting hotspots. By reading all these Operational Agents and accounting for their relationship to the Margin Agent readouts, Proteus analytics platform can effectively provide the source of the issue since in some cases it is a reliability issue that can be traced back to the physics of failure and can be quantified from the stress point of view by the Workload Agent and the Local Thermal Agents, and sometimes can be an environmental issue that can be tracked on a different component in the system such as clock generator or a voltage regulator component for example. This kind of analytics and algorithms performed in the Proteus platform is also known as ‘Agent fusion’.

Fig. 9 shows data from HTOL, this data is similar to what has been seen in real silicon, in a chip in an advanced process node. Before HTOL and during each HTOL readout back at the Automated Test Equipment (ATE), a stress test run over the ICs, and the MA data was extracted at the end of the stress test. In Fig.9 shows the results for one IC, a specific block inside the IC showing 7 MA worse path delay measurements and their degradation over time, after 500 hours of HTOL. Since the MAs cover millions of paths, a comprehensive delay degradation view is established. Delay degradation is different between different ICs, but also different Margin Agents of the same IC show a non-uniform delay degradation and a dependency on the millions of paths under monitor by each Margin Agent as shown in Fig. 9.

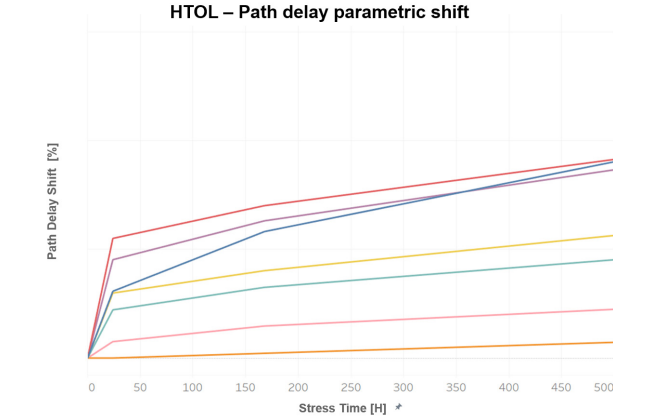


Figure 9: MA readouts during HTOL, plotting path delay degradation of millions of paths over time

Fig. 10 shows a similar picture but this time in a Margin Map view. It shows the measured path delay parametrci shift after 500 hours of HTOL, each point represents a MAs placed in the X and Y coordinates of a specific block inside the IC.

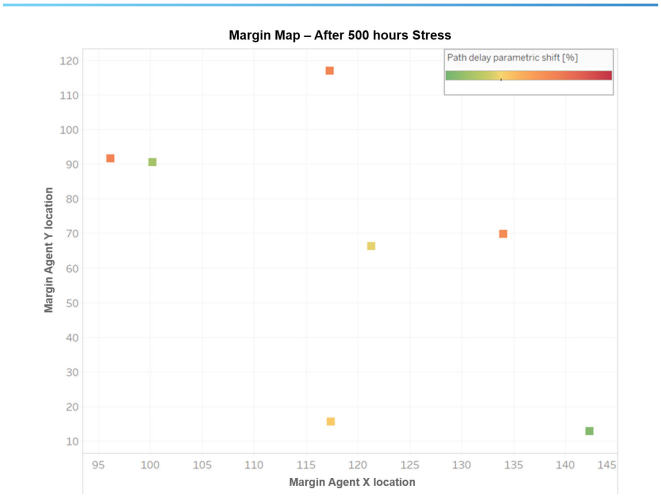


Figure 10:Margin map showing path delay degradation after 500 hours of lifetime acceleration stress (HTOL).

IX. USE CASE: HBM MONITORING

A. Challenge

Visibility of HBM subsystems is limited by nature due to its 3D integration technology, and signal integrity problems are difficult to debug, validate and monitor. Multi-die HBM packaging introduces new reliability challenges which can lead to functional device failures in-field. These technologies are both inherently complex as well as expensive, therefore system failures afflict significant losses on manufacturers and service providers alike.

HBM PHYs do not allow for u-bump redundancies due to the high-density routing, and one u-bump per signal is used for the entire HBM connectivity. A problem in any of the PHY or HBM u-bumps will lead to a chip operational failure. A typical 4xHBM2 includes 13,600 u-bumps for connectivity, creating a reliability challenge and risk of full HBM subsystem failure. In in-field operation, a failure in the HBM subsystem may affect the whole system and lead to an abrupt operational failure and unplanned downtime.

Testing of the HBM subsystem is performed using industry standard detection tools that lack parametric sensitivity so marginal lanes are not detected. These may lead to degradation over time and ultimately failure during in-field operation. Furthermore, detecting faulty lanes requires activation in test mode, therefore degradation over time in mission-mode is not monitored.

As the complexity of heterogenous packaging continues to develop, Proteus's revolutionary approach to HBM in-field monitoring leads to unprecedented reliability assurance. Service providers now have the visibility they need to perform predictive maintenance, detecting and repairing faults in systems before they become failures.

B. Proteus in Action

1) Qualification Stage

The HBM Agent monitors delay degradation during different qualification tests such as baking to model stress migration impact on device degradation, temperature cycling and highly accelerated stress test (HAST) to monitor corrosion impact on device degradation and HTOL to model NBTI, HCI and EM impact on device degradation. The big difference with regular qualification is that now instead of doing pass/fail tests, the HBM Agents based degradation monitoring can show and quantify the degradation experienced by each and every lane, its drivers, receivers and bumps. Based on degradation rates, PoF can be derived and time to failure can be calculated. The Proteus analytics software can correlate the degradation impact of different pins/lanes to placement in the IC, silicon interposer layout and inferred electrical process parameters between others.

The main dominant PoF is communicated and can correlated to the in-field stage to better understand the data analyzed then.

2) In Field Stage

NE and FE signal integrity is simultaneously monitored by the HBM Agents for hundreds of HBM interconnects (covering the whole interconnect path from ASIC to HBM memory) for every chip produced, in mission mode. The results are mapped over time to expose the state of degradation at various resolutions; per chip, per bank, per pin. In addition, at chip production, using the PCA and DPA readouts and the Proteus platform machine learning estimators, the chip can be mapped to a MC corner and RC model; this provides a baseline to compare between chips.

The Proteus platform shows the degradation rates at different scopes, running algorithms in order to decipher the Physics of Failure behind the degradation rate. HBM bumps and I/O buffers reliability are mostly driven by the following mechanisms: stress migration, thermo mechanical fatigue, corrosion, NBTI/HCI, electro-migration. Each of these phenomena is represented by a unique degradation rate [1], once the actual degradation rate is identified then the PoF is identified and the time to failure can be calculated True predictive maintenance may be applied. This may be a timely, scheduled equipment replacement or repair, reducing the costs of acting out of urgency when a failure occurs in the field, or conversely, bringing in the equipment for service periodically, without real need.

In addition, the degradation trends are continually monitored for anomalous phenomena. One example may be observed in **Fig. 11**, where we can see development of a clear and consistent trend over time of the "RX_slope", which is inversely proportional to connectivity integrity. But at around 1000 hours, there is a sharp change in this trend and the slope increases noticeably. Under normal circumstances, such a change would not have been noticeable, until some critical threshold would have been crossed (indicated by the red line), perhaps even only after the lane had failed. However, by analyzing the output of the HBM Agent, the physics-of-failure of the new trajectory provides insight into the new time to failure so predictive maintenance can be applied before a failure occurs.

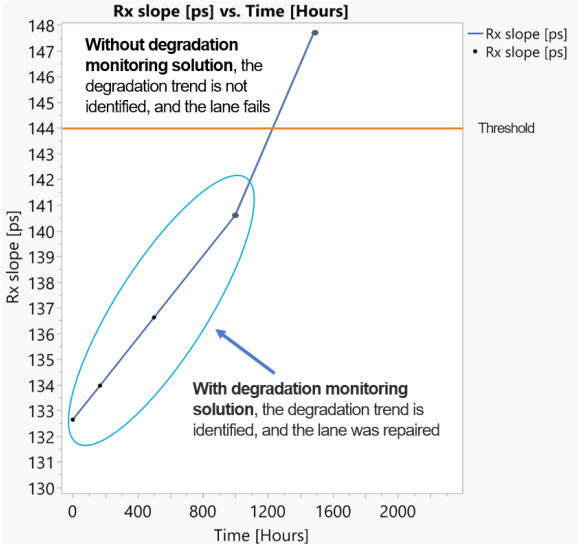


Figure 11: In-Field monitoring and predictive maintenance

In both cases, the consecutive action may be an in-field lane repair. Since the HBM Agent was readout and analyzed in the Proteus platform also at production, the lanes were all graded, and the ones chosen for initial mapping of the signals were the ones with the highest integrity. When degradation triggers the need for a lane repair for whatever reason, the lane grade comes to play again; the repair will be to the best graded lane available, based on production information or re-measured in-field.

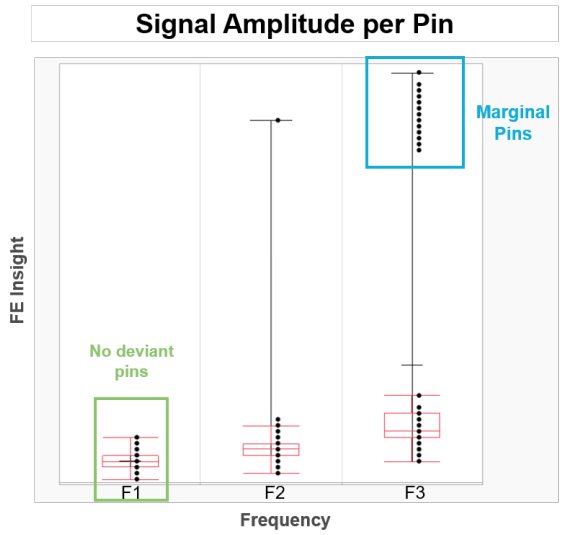


Figure 12: TX parametric characterization during production or In-Field, find the best lane for repair

CONCLUSIONS

Deep Data on-chip monitoring provides unparalleled visibility into electronics, presenting a new realm of reliability science. Putting practice to theory, real-time degradation monitoring provides a basis for time-to-failure modeling, based on the Physics-of-Failure (PoF) mechanisms. Continuously monitoring IC/system critical parameters in-field allows to predict failures and prevent them by alerting the user in advance. This becomes a must-have capability as device designs, materials and manufacturing processes become more complex and reliability challenges increase. This can be achieved today through a unique combination of embedded IPs (Agents) and a software platform that implements machine learning algorithms and data analytics. The Agents monitor at high coverage many areas in the chip, both core and I/O, in conjunction with a software analytics platform that can interpret, infer and analyze this data and generate actionable insights. In-field degradation monitoring allows service providers to control maintenance costs by preempting failures, estimate and extend system life, deploy maintenance and repair resources proactively, reduce operational costs, increase component quality and accelerate root cause analysis. Furthermore, IC/system manufacturers gain visibility at all stages of production allowing them to increase component quality, avoid 'walking wounded' or latent defects, boost manufacturing productivity and reduce costs.

REFERENCES

[1] J. W. McPherson, Reliability Physics and Engineering, 3rd Ed., Springer Publishing, 2019.

[2] Pecht, Michael, Radojcic, Riko; Rao, Gopal. Guidebook for Managing Silicon Chip Reliability (Electronic Packaging), CRC Press. Kindle Edition, 2010

[3] Advanced Materials and Processes Pose Tough Challenges for Electronic Systems Failure Analysis, Eurofins Engineering Sciences White Paper, May 2019

[4] Lau, John H.. 3D IC Integration and Packaging, McGraw-Hill Education. Kindle Edition, 2016

[5] Heterogeneous Integration Roadmap 2019 Edition, Chapter 17: Test Technology, Section 8: System Level Test (http://eps.ieee.org/hir)

[6] Amit Nahar, Kenneth M. Butler, John M. Carulli Jr., Charles Weinberger, Quality Improvement and Cost Reduction Using Statistical Outlier Methods, IEEE 2009

[7] Fan Lin, Chun-Kai Hsu, and Kwang-Ting Cheng, Learning from Production Test Data: Correlation Exploration and Feature Engineering, 2014

[8] J. W. McPherson, Future of Reliability Testing - Can Zero Failures Become a Reality, ESREF Invited Tutorial (2019).

proteanTecs Ltd.
36 Kdoshei Bagdad Dr.
Haifa, Israel 33032
www.proteanTecs.com

proteanTecs